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EXAMINER	
GETACHEW, ABIY	
ART UNIT	**PAPER NUMBER**
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/825,999	ARNOLD ET AL.	
	Examiner	Art Unit	
	Abiy Getachew	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/02/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The 102 rejection based on prior art, Higgins III (US Patent 5,639,989) has been withdrawn. A new ground of rejection has been made in this office action as detailed below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-11 and 14-18, 20-22,25-41are rejected under 35 U.S.C. 102(b) as being anticipated by Kaneko et al. (US Patent 6,476,463 B1).

With respect to claim 1 Kaneko et al teaches a shielded printed circuit board (PCB) (Figure 1) comprising: a PCB comprising a first surface and a second surface; a metallized polymer shield (18B) coupled to the first surface of the PCB; a grounded layer (10B) coupled to the second surface of the PCB; a plurality of conductive vias (6) that extend from the first surface to the grounded layer (10B) so as to electrically couple the metallized polymer shield to the grounded layer (10B), an electronic component mounted to the first surface of the PCB; wherein adjacent conductive vias are spaced within the PCB (Figure 1) a distance that is small enough to reduce a passage of electromagnetic radiation from the electronic component through the spacing between the adjacent conductive vias (6). [Column 1 paragraph 1 lines 6-10]

With respect to claim 3 with all the limitations of claim 1, Kaneko et al teaches wherein the plurality of conductive vias (6), grounded layer (10B), and metallized polymer shield forms a three dimensional grounded EMI shield that substantially envelopes the electronic component (14).

With respect to claim 4 with all the limitations of claim 1, Kaneko et al teaches that the metallized polymer shield is removably coupled to the first surface of the PCB (9).

With respect to claim 5 with all the limitations of claim 4, Kaneko et al teaches that the metallized polymer shield is coupled to the vias through a conductive element (See Figure 1, element 11).

With respect to claims 6 and 21 and with all the limitations of claim 5, Kaneko et al teaches that the conductive element comprises a conductive adhesive (Figure 1, element 16 i.e. a magnetic member 16 of a magnetic material, such as Fe--Ni--Co, is accommodated and secured in position by an adhesive or a solder).

With respect to claims 7 and 20 with all the limitations of claims 4 and 15 respectively, Kaneko et al teaches the metallized polymer shield is coupled to the vias through a mechanical connector (Figure 5, element 30, i.e. as shown in FIG. 5, the multi-chip-module 1 having the construction as described above is mounted in a receptacle 29 having a plurality of flexible connector electrodes 30 connected to the LCC electrodes 11)

With respect to claim 8 with all the limitations of claim 1, Kaneko et al teaches that the PCB (9) comprises two or more layers (See figure 5), wherein the second surface is

between two adjacent layers of the PCB (See figure 5).

With respect to claim 9 with all the limitations of claim 1, Kaneko et al teaches that the second surface (30) is an external, bottom surface of the PCB (32).

With respect to claim 10 with all the limitations of claim 1, Kaneko et al teaches that the grounded layer (10B) comprises a ground plane (8).

With respect to claim 11 and with all the limitations of claim 1, Kaneko et al teaches that the grounded layer (10B) is electrically coupled to a ground plane (8). (See the Abstract, a package substrate 3 has a high frequency transmission line, which is formed by a high frequency circuit layer 8 formed on the surface, a grounding layer 10b formed thereunder and a dielectric ceramic intervening between the layers 8 and 10b)

With respect to claim 14 with all the limitations of claim 1, Kaneko et al teaches an electronic device (See figure 5, it is a device that accomplishes its purpose electronically)

With respect to claim 15 Kaneko et al teaches a printed circuit board (32) comprising: a multi-layered substrate (See figure 5) that comprises a first external surface and a second external surface, wherein a portion of the first external surface is configured to receive an electronic component (Figure. 5, element 5); one or more internal grounded layers (See figure 5) disposed between adjacent layers of the multi-layered substrate; a network of conductive elements (Fig. 1, elements 20) that extend through at least a portion of the multi-layered substrate (See figure 5), wherein the electrically conductive elements extend from at least one of the internal grounded planes to the first external surface; and a shield coupled (18B) to the first surface

(See figure 5), the shield electrically coupled to at least some of the conductive elements to provide an electrical grounding (10b) connection between the shield and the one or more internal grounded planes (18) wherein spaces between adjacent conductive elements (20) comprise a largest dimension that is small enough to substantially reduce emission of electromagnetic radiation from the electronic component. [Column 1 paragraph 1 lines 6-10]

With respect to claim 16 with all the limitations of claim 15, Kaneko et al teaches that the network of conductive elements comprises a plurality of conductively coated (18B).

With respect to claim 17 with all the limitations of claim 15, Kaneko et al teaches a grounding trace (10B) on the first external surface that substantially surrounds the portion of the first external surface that is configured to receive an electronic component (14).

With respect to claim 22 with all the limitations of claim 20, Kaneko et al teaches that the mechanical connector comprises a groove (6) in the first surface, wherein the groove (6) is sized to receive a portion of an EMI shield (5).

With respect to claim 25 and with all the limitations of claim 15, Kaneko et al teaches that the shield (18B) is coupled to a ground trace (8) positioned on the first external surface, wherein the ground trace is in electrical communication with at least some of the conductive elements (See figure 1).

With respect to claim 26 with all the limitations of claim 15, Kaneko et al teaches that the conductive elements (18B) make direct contact with a flange of the shield (15).

(See figure 1)

With respect to claim 27 with all the limitations of claim 26, Kaneko et al teaches a conductive element (18B) is disposed on a portion of the conductive elements (18B) to create an electrical connection to the shield positioned on the first external surface. (Kaneko et.al. teaches that the multi-chip-module is connected to a printed circuit board as a mounting substrate by forming solder balls on an electrode pad provided on the ceramic package and connecting the ceramic package via the solder ball to the printed circuit board)

With respect to claim 28 with all the limitations of claim 26, Kaneko et al teaches that the conductive element (18B) comprises conductive adhesive. [Column 3 paragraph 6 lines 47-54]

With respect to claim 29 with all the limitations of claim 15, Kaneko et al teaches an electronic device comprising the PCB of claim 15. (See figure 5, it is a device that accomplishes its purpose electronically)

3. With respect to claim 30 Kaneko et al teaches a method of shielding an electronic component on a printed circuit board (PCB), the method comprising: providing a PCB (32) that comprises an electronic component (14) on a first surface of the PCB (32) and one or more grounded layers, and a plurality of conductive vias (6) that extend from the coupling a metallized polymer shield to the first surface of the PCB (32) and around the electronic component to create an electrical connection to the conductive vias and the grounded layer (10B) wherein the electrical connection between the grounded layer(s), vias, and the metallized polymer shield forms a grounded EMI

shield that substantially surrounds the electronic component(14) wherein adjacent conductive vias are spaced within the PCB (32) a distance that is small enough to reduce a passage of electromagnetic radiation from the electronic component through the spacing between the adjacent conductive vias (6) [Column 1 paragraph 1 lines 6-10].

With respect to claim 31-33 with all the limitations of claim 33 Kaneko et al teaches comprising placing the PCB in a housing of an electronic device. (See figure 5, it is a device that accomplishes its purpose electronically)

With respect to claim 34-36 with all the limitations of claim 30 Kaneko et al teaches comprising positioning a conductive adhesive between the metallized polymer shield and the first surface before the metallized Dolvmer shield is coupled to the first surface of the PCB. (See figure 1, element 16 i.e. a magnetic member 16 of a magnetic material, such as Fe--Ni--Co, is accommodated and secured in position by an adhesive or a solder).

With respect to claim 37 with all the limitations of claim 30 Kaneko et al teaches wherein at least one of the grounded layers (8) comprises a ground plane (See figure 5).

With respect to claim 38 with all the limitations of claim 30 Kaneko et al teaches wherein providing a PCB (32) comprises forming a groove (6) in the first surface of the PCB (32).

With respect to claim 39 with all the limitations of claim 1 Kaneko et al teaches wherein at least one of said conductive vias (6) is located below said PCB (32).

With respect to claim 40 with all the limitations of claim 15 Kaneko et al teaches wherein at least one of said conductive elements (Fig. 1, elements 20) is located below said electronic component (14).

With respect to claim 41 with all the limitations of claim 30 Kaneko et al teaches wherein said providing a PCB (32) further comprises providing at least one of said plurality of conductive vias (6) to be located below said PCB (32).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12,13,23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins.

With respect to claim 12 and 24 with all the limitations of claim 1 and 15 respectively, Higgins teaches all of the limitations except that a metal layer is disposed over at least one surface of the shaped polymer substrate. Metal layers in the shielding art and PCB art are well known, they are used for the shielding itself or for structural support. It would have been obvious to one of ordinary skill in the art at the time of the invention add a metal layer disposed on a surface of the shaped polymer substrate for the purpose of adding structural strength while increasing the shielding capability of the structure.

With respect to claim 13 and with all the limitations of claim 1, Higgins teaches all of the limitations except for that the flange comprises openings. When attaching a component to a circuit board we need the component connectors to make physical contact with the vias structures on the board, in order to do this there must be openings in any material that covers the vias. It would have been obvious to one of ordinary skill in the art at the time of the invention to have openings on the flange for the purpose of attaching more components to the vias underneath.

With respect to claim 23 and with all the limitations of claim 15, Higgins teaches all of the limitations except that the shield comprises a metal can. Metal cans are well known in the shielding art and are used in various realms to shield devices from EMI emissions while at the same time providing structural strength for physical protection of the device. It would have been obvious to one of ordinary skill in the art at the time of the invention add a metal can disposed on a surface of the shaped polymer substrate for the purpose of adding structural strength while increasing the shielding capability of the structure.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higgins in view of Kaneko (US Patent 6476463).

With respect to claim 19 and with all the limitations of claim 18, Higgins teaches all of the limitations except does not teach specifically that the largest dimension is smaller than half a wavelength of EMI emissions from the electronic component. Kaneko teaches vias that are separated by certain dimensions wherein the largest dimension is smaller than half a wavelength of EMI emissions from the electronic

component (column 5, lines 13-17). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the largest dimension separating vias to be smaller than half a wavelength of EMI emissions from the electronic component, for the purpose of quickly attenuating the EMI emissions.

Relevant Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Furman et al. (US 6,732,908 B2) teaches fabricating extremely small semiconductor devices and current, commonly referred to as "chips." And Mathews et al. (US 6,686,649 B1) Multi-chip semiconductor package with integral shield and antenna

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abiy Getachew whose telephone number is (571) 272 6932. The examiner can normally be reached on Monday to Friday 8Am to 4:30Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Abiy Getachew
Examiner
Art Unit 2841

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July 9, 2007

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7/23/07